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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,165	10/14/2004	Shiro Sakiyama	71971-015	6689

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EXAMINER	
HILTUNEN, THOMAS J	
ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/511,165	SAKIYAMA ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-12 and 15-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-17* is/are allowed.

6)☒ Claim(s) *6-9 and 11* is/are rejected.

7)☒ Claim(s) *10 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's request for consideration filed 30 April 2008 has been received and entered in the case. The claims filed 30 April 2008 are considered below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over So et al. (USPN 5,883,544) in view of Miyazaki et al. (USPN 6,466,077).

With respect to claim 6, So et al. discloses in Fig. 1, a semiconductor integrated circuit, comprising:

a main circuit (PMOS transistors 13 of 10b) including a plurality of MOS transistors (PMOS transistors13) in which a source potential and a substrate potential are separated from each other (the substrate and source potentials are separate), and operating while receiving an operating power supply voltage (PMOS transistors must receive an operating power supply voltage, i.e., VDD or the like, otherwise the transistors would be inoperative); and

a substrate potential control circuit (circuit of 10B lest the PMOS transistors 13) for controlling the substrate potential of a MOS transistor in the main circuit (the substrate potential control circuit controls the substrate potential of PMOS transistors 13

via the VBIAS' signal) so that an actual a saturation current value of the MOS transistor is equal to a target saturation current value (VBIAS controls the substrate of 13 to the target threshold/saturation current of PCH1), the substrate potential control circuit, including:

a constant current generation circuit (NCH1 generating Ids');

a current-voltage conversion circuit (PCH1) including a MOS transistor provided therein (PCH1) and having current-voltage conversion characteristics that change according to the substrate potential of the MOS transistor provided therein for converting a constant current value of the constant current generation circuit to a voltage value (PCH1 operates as recited to convert Ids' to VD'); and

a differential amplifier circuit (PCH2, PCH3, PCH4, NCH2 and R1) comparing the voltage value generated by the current-voltage conversion circuit (VD') with a reference voltage (VR') and outputting a voltage (VBIAS' based on Vo') for controlling the substrate potential of the current-voltage conversion circuit so that the voltage value generated by the current-voltage conversion circuit is equal to the reference voltage (the differential amplifier operates to control VD' to equal VR', see Col. 5 lines 18-20 and lines 49-56),

wherein the substrate potential control circuit controls a substrate potential of a MOS transistor in the main circuit (VBAIS' controls the substrate potential of the PMOS transistors 13).

Note, So et al. discloses that VR' may be supplied by resistive divider (R3' and R2'), however So et al. further discloses that VR' may be supplied via a pin 16'. VR'

may be any desired voltage that is required to be provided to the substrate of PMOS transistors 13 and PCH1.

So et al. fails to specifically disclose, that VR' is "equal to the operating power supply voltage of the main circuit". Thus So et al. fails to disclose the differential amplifier comparing the "voltage value generated by the current-voltage conversion circuit with the operating power supply voltage" and "the voltage value generated by the current-voltage conversion circuit is equal to the operating power supply voltage of the main circuit". However, it is old and well known to control the substrate voltage of a PMOS transistor so that is equal to its operating supply voltage for the purpose of optimizing the transistor's performance with respect to operation speed and leakage current. For instance, the higher a substrate potential of a PMOS transistor is, i.e., above the operating supply potential, the slower the transistor will operate/switch, however its leakage current will decrease. Conversely, the lower substrate potential of a PMOS transistor, i.e., at or below the operating power supply, the faster the transistor will operate, however its leakage current will increase. As one of ordinary skill in the art would understand the substrate potential of a transistor is selected based on a trade off between operation speed and leakage current. Thus by biasing a PMOS transistor to its operating supply voltage the PMOS transistor will be controlled to be in a "normal" operating condition that is optimized by the trade off between switching speed and leakage current. This is further evidenced by Miyazaki et al. in Fig. 32 which discloses such a stand by, i.e., low leakage current where the substrate is above Vdd, normal,

i.e., substrate voltage at supply potential Vdd, and forward bias states, i.e., faster operation higher leakage current where the substrate is below Vdd.

It would have been obvious to one of ordinary skill in the art at the time of the invention to input the operating substrate voltage of PMOS transistors 13 as VR' so that VD' and VBIAS' will become equal to the operating substrate voltage due to the forced feedback of the circuit of 10b, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). One of ordinary skill in the art would have been motivated to supply the operating supply voltage to VR' in order to bias the PMOS transistors 13 to their operating supply voltage to optimize the PMOS transistors' operating characteristics with respect to desired operation speeds and leakage currents.

With respect to claim 7, the above modification discloses, the semiconductor integrated circuit of claim 6, wherein the constant current value of the constant current generation circuit is dependent on the operating power supply voltage (NCH1 has its gate connected to VDD, thus it is dependent upon the power supply voltage).

With respect to claim 8, the above modification discloses, the semiconductor integrated circuit of claim 6, the constant current value of the constant current generation circuit is in a linear function relationship with the operating power supply voltage value (the circuit of Fig. 1b is connected as recited and therefore must operate as recited. Furthermore, above limitation is merely a functional limitation which the circuit of Fig. 10b is capable of performing).

With respect to claim 9, the above modification discloses, the semiconductor integrated circuit of claim 6, wherein:

the main circuit has a plurality of operating power supply voltage ranges (the power supply voltage supplied to 13 may be any of a number of supply voltage values, thus the circuit has ;

the constant current value of the constant current generation circuit is in a linear function relationship with an operating power supply voltage value within an operating voltage range for each operating power supply voltage range of the main circuit (the circuit will have a linear output with any selected operating power supply voltage); and

the linear function relationship between the constant current value of the constant current generation circuit and the operating power supply voltage value is different for each operating power supply voltage range (changing the supply voltage input to the circuits will change the values, i.e., linear relationships, between each of the selected values).

With respect to claim 11, the above modification discloses, the semiconductor integrated circuit of claim 6, wherein the constant current generation circuit generates a constant current with a variation rate smaller than that for the saturation current value of the MOS transistors of the main circuit (the above limitation is merely a functional limitation that does not structurally limit the claim. NC11 is capable of being operated as recited).

Allowable Subject Matter

Claims 10 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 10, there is no cited art that discloses, the constant current source generating a plurality of constant current values and selectively outputting one of the constant current values in the circuit as recited in claim 6. Clearly, So et al. discloses only outputting one constant current value IDS'.

With respect to claim 12, there is no cited art that discloses, the constant current generation circuit including an adjustment circuit for reducing variations in the generated constant current value in combination with the circuit as recited in claim 11. So et al. fails to disclose such an "adjustment circuit", nor is there any seen motivation for adding such a circuit.

Claims 15-17 are allowed.

With respect to claim 15, clearly it can be seen that Kaenel et al. does not disclose "the target saturation current value of the MOS transistors of the main circuit is in a linear function relationship with the operating power supply voltage supplied to the main circuit". In fact, Fig. 10 discloses a logarithmic relationship between the current and supply voltage. Thus Kaenel et al. teaches away from a linear relationship between the saturation current and the supply voltage. Furthermore, there is no disclosure or motivation provided to have a linear relationship between the supply voltage and saturation current. It can be seen that Tang et al. discloses in Fig. 5 a linearly

relationship between supply voltage bias voltage, and Vout'. Thus, the saturation current and supply voltage would have an inherent linear relationship. However, Tang fails to disclose the specific "power supply voltage control circuit" of as recited in claim 13. Thus, Tang fails to disclose all the recited limitations of claim 15. Therefore, claim 15 is allowable.

With respect to claim 16, it can be seen that claim 16 recites the same linear relationship between the target saturation current value and the operating power supply voltage value of claim 15. Thus, claim 16 is allowable for at least the same reasons as claim 15.

Response to Arguments

Applicant's arguments with respect to claims 6-9 and 11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on M-F 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571)272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TH
June 20, 2008

/N. Drew Richards/
Supervisory Patent Examiner, Art Unit 2816